Listing of Claims

1-30 (Canceled)

31. (New) A semiconductor device, comprising:

a first set of signal wires distributed among at least first and second adjacent layers; and

a second set of signal wires distributed among at least the first and second layers, the first and second sets having a different number of signal wires, with the signal wires in the first set being substantially parallel and arranged in a first pattern, and the signal wires in the second set being substantially parallel and arranged in a second pattern.

32. (New) The semiconductor device of claim 31, wherein each of the first and second sets have an even number of signal lines.

33. (New) The semiconductor device of claim 31, wherein the first layer has a number of signal wires from the first and second sets different from a number of signal wires from the first and second sets in the second layer.

34. (New) The semiconductor device of claim 31, wherein the first and second patterns are a same pattern.

35. (New) The semiconductor device of claim 31, wherein the first pattern is different from the second pattern.

36. (New) The semiconductor device of claim 31, wherein the first and second patterns are alternating patterns.

37. (New) The semiconductor device of claim 31, wherein the number of signal wires in the first layer of the first set is different from the number of signal wires in the first layer of the second set.

38. (New) The semiconductor device of claim 31, wherein the signal wires in the first set are distributed in an alternating pattern among the first and second layers, and the signal wires in the second set are distributed in an aligned pattern among the first and second layers.

39. (New) The semiconductor device of claim 31, wherein the first and second layers are adjoining layers.

40. (New) The semiconductor device of claim 31, wherein the signal wires in at least one of the first and second sets are distributed among the first and second layers and at least a third layer adjacent the first and second layers.

41. (New) The semiconductor device of claim 40, wherein the first, second, and third layers are adjoining layers.

42. (New) The semiconductor device of claim 31, wherein the signal wires in the first and second sets are distributed among the first and second layers and at least a third layer adjacent the first and second layers.

43. (New) The semiconductor device of claim 41, wherein the signal wires in the first and second sets are distributed in a same type of pattern among the first, second, and third layers.

44. (New) The semiconductor device of claim 43, wherein the same type of pattern is an alternating pattern.

45. (New) The semiconductor device of claim 42, wherein the signal wires in the first and second sets are distributed in different patterns among the first, second, and third layers.

46. (New) The semiconductor device of claim 45, wherein the different patterns are different alternating patterns.

47. (New) The semiconductor device of claim 42, wherein the first, second, and third layers are adjoining layers.

48. (New) The semiconductor device of claim 31, wherein signal wires in the first layer are local interconnect wires and signal wires in the second layer are global routing wires.

49. (New) The semiconductor device of claim 31, wherein the signal wires in the first set have a same permittivity and the signal wires in the second set have a same permittivity.

50. (New) The semiconductor device of claim 31, wherein the first set of signal wires is separated from the second set of signal wires.

51. (New) The semiconductor device of claim 50, wherein the first set of signal wires is separated from the second set of signal wires by one or more ground or return wires.

52. (New) The semiconductor device of claim 51, wherein the first set of signal wires is separated from the second set of signal wires by ground or return wires in the first and second layers.

53. (New) The semiconductor device of claim 52, wherein the first set of signal wires is located between the one or more ground or return wires and one or more power supply wires.

54. (New) The semiconductor device 53, wherein the second set of signal wires is located between the one or more ground or return wires and one or more additional power supply lines.

55. (New) The semiconductor device of claim 54, wherein the signal wires from the first and second sets located in the first layer are between first and second power supply lines in the first layer.

56. (New) The semiconductor device of claim 55, wherein the signal wires from the first and second sets that are located in the second layer are between third and fourth power supply lines in the second layer.

57. (New) A semiconductor device, comprising:

a first set of signal wires distributed among at least first and second adjacentlayers; and

a second set of signal wires distributed among at least the first and second layers, the signal wires in the first set being substantially parallel in a first direction, the signal wires in the second set of the first layer being substantially parallel in the first direction, and the signal wires in the second set of the second layer being in a second direction different from the first direction.

58. (New) The semiconductor device of claim 57, wherein the first and second directions are at least substantially orthogonal directions.

59. (New) The semiconductor device of claim 57, wherein the first and second sets have a different number of signal wires.

60. (New) The semiconductor device of claim 57, wherein the signal wires in the second set of the second layer are located in an area free from frequency limiting paths.

61. (New) A system comprising:

a first circuit having an interconnect structure that includes:

(a) a first set of signal wires distributed among at least first and second adjacent layers; and

(b) a second set of signal wires distributed among at least the first and second layers, the first and second sets having a different number of signal wires, with the signal wires in the first set being substantially parallel to one another and arranged in a first pattern, and the signal wires in the second set being substantially parallel to one another and arranged in a second pattern.

62. (New) The system of claim 61, wherein the first circuit is a processor.

63. (New) The system of claim 62, wherein the processor sends signals to a second circuit through the interconnect structure, the second circuit corresponding to at least one of a memory, a cache, a network interface, a chipset, a graphical interface, and a power supply.

64. (New) The semiconductor device of claim 31, wherein the signal wires in at least one of the first and second sets are in a non-overlapping relationship with one another.